What is claimed is:

1. An ATM buffer system comprising:

a configurable buffer circuit to store a plurality of ATM linked lists; and

a linked list monitor to monitor the plurality of ATM linked lists, wherein the linked list monitor is configurable to monitor different length linked lists.

2. The ATM buffer system of claim 1 wherein the configurable buffer circuit comprises:

insert logic to insert ATM cells into the plurality of ATM linked lists; and

extract logic to remove the ATM cells from the plurality of ATM linked lists.

3. The ATM buffer system of claim 2 wherein the configurable buffer circuit further comprises first and second state machines to control the insert logic and the extract logic, respectively.

4. The ATM buffer system of claim 1 wherein the linked list monitor comprises:

a plurality of counter circuits:

a plurality of comparator circuits coupled to the plurality of counter circuits, the plurality of comparator circuits compare a count from the plurality of counter circuits to first and second threshold values; and

control circuitry coupled to the plurality of comparator circuits to selectively increment or decrement the count of the plurality of counter circuits.

5. The ATM buffer system of claim 4 wherein the control circuitry selectively controls the plurality of comparator circuits in response to a configuration of the buffer circuit.

6. The ATM buffer system of claim 4 wherein the first threshold value is an overflow threshold selected to correspond to a maximum length of an ATM linked list

stored in the buffer circuit, and second threshold value is a cell loss priority (CLP) threshold selected to correspond to a desired list length based on a priority of ATM cells.

7. The ATM buffer of claim 1 further comprising a general monitor circuit coupled to monitor the buffer circuit.

8. The ATM buffer of claim 7 wherein the general monitor circuit comprises:

an undefined bit rate (UBR) counter to count a number of UBR ATM cells stored in the buffer;

an constant bit rate (CBR) counter to count a number of CBR ATM cells stored in the buffer; and

a cell counter to count a total number of ATM cells stored in the buffer.

9. The ATM buffer of claim 8 wherein the general monitor circuit comprises:

a CLP counter to count a number of non-priority ATM cells dropped from the buffer; and

an overflow counter to count a number of ATM cells dropped from the buffer in response to an overflow condition.

10. The ATM buffer of claim 8 further comprising:

first and second comparators to compare the count of the undefined bit rate (UBR) counter to a UBR cell loss priority (CLP) threshold value and a UBR overflow threshold, respectively;

third and fourth comparators to compare the count of the constant bit rate (CBR) counter to a CBR cell loss priority (CLP) threshold value and a CBR overflow threshold, respectively; and

fifth and sixth comparators to compare the count of the overflow counter to a buffer cell loss priority (CLP) threshold value and a buffer overflow threshold, respectively.

11. The ATM buffer of claim 1 wherein the plurality of ATM linked lists have an associated priority status, and the linked list monitor comprises configurable threshold values based upon the priority status of the plurality of ATM linked lists.

12. A linked list buffer system comprising:

a buffer having a plurality of data storage locations, wherein the buffer can store a plurality of different linked list configurations; and

a management system coupled to the buffer and comprising a plurality of counter circuits having adjustable threshold values, wherein the adjustable threshold values can be programmed to correspond to the plurality of different linked list configurations of the buffer.

13. The linked list buffer system of claim 12 wherein the adjustable threshold values comprise an overflow threshold value and a cell loss priority threshold value.

14. The linked list buffer system of claim 12 wherein the plurality of different linked list configurations comprises one, two, eight, ten or sixteen linked lists.

15. The linked list buffer of claim 14 wherein the plurality of counter circuits comprises sixteen counters and comparator circuits.

16. An asynchronous transfer mode (ATM) buffer system comprising:

a universal test and operations interface (UTOPIA) output connection;

a low voltage differential signal (LVDS) input connection;

a buffer circuit coupled between the LVDS input connection and the UTOPIA output connection, the buffer circuit comprises insert logic to insert ATM cells into the plurality of ATM linked lists stored in the buffer circuit, and extract logic to remove the ATM cells from the plurality of ATM linked lists;

a linked list monitor coupled to the buffer circuit and comprising a plurality of first counter circuits, a plurality of comparator circuits coupled to the plurality of first

counter circuits, the plurality of comparator circuits compare a count from the plurality of first counter circuits to first and second threshold values, and control circuitry coupled to the plurality of comparator circuits to selectively increment or decrement the count of the plurality of first counter circuits.

17. The asynchronous transfer mode (ATM) buffer system of claim 16 wherein the first threshold value is an overflow threshold selected to correspond to a maximum length of an ATM linked list stored in the buffer circuit, and second threshold value is a cell loss priority (CLP) threshold selected to correspond to a desired list length based on a priority of ATM cells.

18. The asynchronous transfer mode (ATM) buffer system of claim 16 further comprising a general monitor circuit coupled to monitor the buffer circuit, wherein the general monitor circuit comprises:

an undefined bit rate (UBR) counter to count a number of UBR ATM cells stored in the buffer;

an constant bit rate (CBR) counter to count a number of CBR ATM cells stored in the buffer; and

a cell counter to count a total number of ATM cells stored in the buffer.

19. The asynchronous transfer mode (ATM) buffer system of claim 17 further comprising:

first and second comparators to compare the count of the undefined bit rate (UBR) counter to a UBR cell loss priority (CLP) threshold value and a UBR overflow threshold, respectively;

third and fourth comparators to compare the count of the constant bit rate (CBR) counter to a CBR cell loss priority (CLP) threshold value and a CBR overflow threshold, respectively; and

fifth and sixth comparators to compare the count of the overflow counter to a buffer cell loss priority (CLP) threshold value and a buffer overflow threshold, respectively.

20. A method of operating an ATM buffer comprising:

configuring the ATM buffer to store a plurality of linked lists;

establishing ATM cell length thresholds for the plurality of linked lists; and

configuring a monitor circuit coupled to the ATM buffer to monitor the plurality of linked lists using the ATM cell length thresholds.

21. The method of claim 20 wherein the ATM cell length thresholds comprise an overflow threshold value equal to a maximum length of the plurality of linked lists, and a cell loss priority threshold value that is less than the overflow threshold value.

22. The method of claim 20 wherein the monitor circuit comprises a plurality of selectable counter circuits and comparator circuits, wherein during operation the comparator circuits receive the ATM cell length thresholds and compare the ATM cell length thresholds to a count in the counter circuits.

23. The method of claim 20 wherein the plurality of linked lists comprises either one, two, eight, ten or sixteen linked lists.

24. A method of operating an ATM buffer comprising:

receiving an ATM cell comprising a header and data, wherein the header includes an indication of a priority level of the ATM cell;

incrementing a count value of linked list length stored in the ATM buffer;

comparing the count value to a linked list length overflow threshold value;

determining if the count value exceeds the linked list length overflow threshold value;

comparing the count value to a linked list length priority threshold value; and

determining if the count value exceeds the linked list length priority threshold value.

25. The method of claim 24 further comprising storing the ATM cell in the ATM buffer if count value does not exceed the linked list length overflow threshold value or the linked list length priority threshold value.

26. The method of claim 24 further comprising storing the ATM cell in the ATM buffer if count value does not exceed the linked list length overflow threshold value, and the ATM cell is a priority cell.

27. The method of claim 24 further comprising not storing the ATM cell in the ATM buffer if count value exceeds the linked list length overflow threshold value, or count value exceeds the linked list length priority threshold value and the ATM cell is a low priority cell.

28. The method of claim 24 further comprising:

configuring the ATM buffer to store a plurality of linked lists; and

selecting the linked list length overflow threshold value and the linked list length priority threshold value based upon the plurality of linked lists.